UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/945,394 | 08/30/2001 | Steve Van Kirk | 303.755US1 | 3192 |

21186 7590 11/04/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

| EXAMINER | |
|---|---|
| DINH, TUAN T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2841 | |

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/945,394 | KIRK, STEVE VAN | |
| | Examiner | Art Unit | |
| | Tuan T Dinh | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) *5-19,21-27,31-33,39-42 and 49-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,20,28-30,34-38,43-48 and 65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 20, 28, 38, 43, and 65, are rejected under 35 U.S.C. 102(b) as being anticipated by Kumagai et al. (U. S. Patent 6,147,573).

As to claims 1-4 28, 38, Kumagai et al. discloses a circuit board (24,column 4, line 67 as a multilayer structure of a electronic part, i.e. capacitor, inductor...) as shown in figures 1A-1E comprising:

first and second conductive layer (terminal electrodes, 20, column 4, line 34) including first and second interstices (29, column 4, line 54), and a dielectric layer (1, column 4, lines 15-16) disposed between the first and second interstices (29), the terminal electrodes (20) are inherently as positive and negative electrodes as consider power and ground electrodes, terminals, or planes.

As to claim 65, Kumagai et al. discloses a circuit board having first and second conductive layers (20) as shown in figures 1-3 comprising:

means for forming a first interstice (29) in the first conductive layer (20);

means for forming a second interstice (29) in the second conductive layer (20);

means for inserting a dielectric layer (1) between the first and second interstices; and

means for engaging the first and second interstices by the dielectric layer (24).

As to claim 20, Kumagai et al. discloses a circuit board as shown in figures 3B-3C comprising:

first and second conductive layers (20) including first and second interstices (29), wherein the first interstice has a plurality of first widths laying in a first plane, see figure 3B the width of the first interstice wounded around and parallel with the surface of the conductor layer 20; the second interstice (29) engaged with the first interstice by a dielectric layer (1) disposed between the first and second interstices (29), wherein the second has a second width laying in a second plan; the first and second planes are substantially parallel, and wherein the second width is substantially overlaps at least one of the plurality of the first width, see figure 3B.

As to claim 43, Kumagai et al. discloses first and second conductive layers (20) are vertically-overlapping (see figure 3B), and wherein the first interstice has a plurality of width laying a first plane and the second interstice has a second width laying in a second plane, and the planes are substantially parallel, and wherein the second width substantially overlaps at least one of the plurality of the first width (see figure 3B).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagai et al. ('573) in view of Takaya et al. (U. S. Patent 6,713,162).

Regarding claims 29-30, Kumagai et al. discloses the dielectric layer (1), except for the dielectric constant about 3 to 5.

Takaya et al. shows the dielectric layer (10a-10e), see figures 1-2, having a dielectric constant about 3-5 (e=2.6-3.5, column 15, lines 20-21).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a dielectric layer having a dielectric constant about 3-5 in the circuit board of Takaya et al., as taught by Kumagai et al., for the purpose of reducing a power supply impedance and increasing charge storage in the dielectric layer.

5. Claims 34-37, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagai et al. ('573) in view of Lee et al. (U. S. Patent 5,497,037).

As to claims 34-37, Kumagai et al. discloses a circuit board as shown in figures 1-3 having first and second conductive layers (20), wherein the first and second conductive layer (20) include first and second interstice (29), the circuit board comprising:

a capacitor having a dielectric layer (1, because the dielectric layer formed between the two terminals (20)) disposed between and engaged the first and second interstices (29). Kumagai et al. does not disclose an electrical circuit mounted on the circuit board and powered by a first power supply voltage. Lee et al, which discloses power supply voltages (105) having 3.3V connected to a cap (108) and first and second conductive layers (103, 104), see figure 4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a circuit connected to a power supply as taught by Lee, applied in the circuit board of Kumagai for the purpose of providing DC and AC power supply voltages.

As to claim 44, Nakao et al. discloses al of the limitations of the claimed invention, except for first and second power supplies connected to the first and second conductive layers. Lee et al shows a printed circuit board (PCB) in figures 2 and 4 comprising first and second power supplies (16-figure 2) or (105-figure 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize two power supplies in the system of Kumagai et al, as taught by Lee et al. in for the purpose of providing DC/DC or DC/AC voltage power.

6. Claims 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagai et al. ('573) in view of Takeshita et al. (US 6,469,259).

Regarding claims 45-46, Kumagai et al. discloses all of the limitations as explained in claims 1-4, except for component, which is connected to the first and second conductive layers (or power and ground planes), is a memory chip or processor.

Takeshita et al. shows a wiring board comprising a semiconductor device (4), which is an IC or LSI connected to power and ground layers (5,6), see column 5, lines 10-19.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a memory chip or a processor in the memory circuit module or a computer system of Kumagai et al, as taught by Takeshita et al., for the purpose of providing high frequency current.

As to claims 47-48, Kumagai et al discloses the first and second interstices are formed in complementary or complementary rectangular shapes, see figure 3B.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-4, 20, 28-30, 34-38, 44-48, and 65 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues Nakao ('377) does not disclose claimed invention. Examiner agrees. The previous Office action is hereby withdrawn.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Breen and Person et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
September 29, 2004.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800